

REMARKS

Claims 1-7, 9-18, and 20-22 are presently pending in the instant application. The Examiner has objected to claims 1 and 12 due to informalities. Claims 1-3, 5-7, 9-10, 12-14, 16-18, and 20-21 have been rejected under 35 U.S.C. 102(b) as allegedly being anticipated by U.S. Patent No. 5,471,591 to Edmondson et al. (Edmondson). Also, claims 4, 11, 15, 17, 18, and 22 have been rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Edmondson in view of a document by Hennessy. Claims 1, 2, 9, 12, 13, 20, and 21 have been amended. The Applicants submit that the instant application is in condition for allowance for at least the reasons set forth below. No new matter has been entered.

Claim Objections

Claims 1 and 12 were objected to because of informalities. The Applicants have amended claims 1 and 12 to incorporate the Examiner's suggestion, namely, revising the phrase "...updated during a operand prefetching period..." to recite "...updated during an operand prefetching period..." in order to reflect the proper article "an".

35 USC 102

Claims 1-3, 5-7, 9-10, 12-14, 16-18, and 20-21 have been rejected under 35 U.S.C. 102(b) as allegedly being anticipated by Edmondson. Applicants' amended claim 1 recites a method for "holding up operands of R-unit registers for a minimum number of cycles until all prior updates have completed by comparing addresses of said R-unit registers in at least one queue and interlocking valid matches of said R-unit register addresses, the method comprising:

receiving a plurality of R-unit register addresses associated with a millicode architecture environment, said R-unit register addresses including at least one of a millicode general register

and a millicode access register;

storing said R-unit register addresses in a plurality of queues;

accessing said queues;

comparing said R-unit register addresses;

determining matches between said R-unit register addresses; and

implementing one or more write-before-read interlocks after said determining produces a valid match, said one or more write-before-read interlocks being implemented until said comparing is no longer active, whereby operands of R-unit registers are updated during an operand prefetching period with a minimum number of cycles."

Edmondson does not recite these features. Specifically, Edmondson does not teach or suggest a millicode architecture-based method and system for executing the functions recited in Applicants' claim 1. Further, Edmondson does not teach or suggest a recovery unit, or R-unit, but rather recites a scoreboard, which as described in the Edmondson reference, performs various functions relating to general purpose registers, access registers, and floating point registers provided in a standard processing environment (col. 1, lines 35-57; col. 3, lines 25-34; and col. 4, lines 20-43). The R-unit recited in Applicants' claim 1 is specific to the millicode architecture and supports multiple registers not supported by the scoreboard recited in the Edmondson reference. The R-unit recited in the Applicants' amended claim 1 performs functions relating to millicode instructions and registers including a millicode access register and a millicode general register that are specific and unique to a millicode architected processing environment. Thus, the scoreboard and associated elements of the Edmondson reference are not equivalent to the R-unit and millicode processing environment as provided in Applicants' claim 1. Accordingly, the Applicants submit that claim 1 is patentable over Edmondson. Reconsideration of the rejection is respectfully requested.

Applicants' amended claim 12 recites a "system holding up operands of R-unit registers for a minimum number of cycles until all prior updates have completed by comparing addresses of said R-unit registers in at least one queue and interlocking valid matches of said R-unit register addresses, the system comprising:

a plurality of queues for storing R-unit register addresses associated with a millicode

architecture environment, said R-unit register addresses including at least one of a millicode general register and a millicode access register;

a comparator for comparing said R-unit register addresses in said plurality of queues and determining matches between said R-unit register addresses; and

a plurality of write-before-read interlocks that are implemented after valid matches of said R-unit register addresses are determined, said write-before-read interlocks being implemented until said comparing is no longer active, whereby operands of R-unit registers are updated during an operand prefetching period with a minimum number of cycles."

The Applicants' submit that amended claim 12 is patentable over Edmondson for at least the reasons provided above with respect to claim 1. Claims 2, 3, 5-7, and 9-10 depend from what is an allowable claim 1. Claims 13, 14, 16-18, 20, and 21 depend from what is an allowable claim 12. For at least these reasons, claims 2, 3, 5-7, 9, 10, 13, 14, 16-18, 20, and 21 are patentable over Edmondson. The Applicants request reconsideration of the outstanding rejections.

Notwithstanding, claims 2, 9, 13, and 20 have been amended to clarify that the read instruction is a millicode instruction.

35 USC 103

Claims 4, 11, 15, 17, 18, and 22 have been rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Edmondson in view of Hennessy. The Applicants' claims 4 and 11 are dependent upon an allowable claim 1. Claims 15, 17, 18, and 22 are dependent upon an allowable claim 12. For at least these reasons, the Applicants submit that claims 4, 11, 15, 17, 18, and 22 are in condition for allowance and respectfully request reconsideration of the outstanding rejections.

In view of the foregoing, it is respectfully submitted that the instant application is in condition for allowance. Accordingly, it is respectfully requested that this application be allowed and a Notice of Allowance issued. If the Examiner believes that a telephone conference with

Applicant's attorneys would be advantageous to the disposition of this case, the Examiner is cordially requested to telephone the undersigned.

In the event the Commissioner of Patents and Trademarks deems additional fees to be due in connection with this application, Applicant's attorney hereby authorizes that such fee be charged to Deposit Account No. 09-0463.

Respectfully submitted,

CANTOR COLBURN LLP

By Marisa J. Dubuc
Marisa J. Dubuc
Registration No. 46,673
Customer No. 23413

Date: May 27, 2004
Address: 55 Griffin Road South, Bloomfield, CT 06002
Telephone: (860) 286-2929